REMARKS/ARGUMENTS

Favorable consideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-6 are pending in the application, with Claims 1, 2 and 5 amended and Claims 7-18 cancelled by the present amendment.

In the outstanding Office Action, Claims 7-18 were withdrawn from consideration; Claims 1, 2 and 5 were objected to; Claims 1-4 and 6 were rejected under 35 U.S.C. § 102(e) as being anticipated by Noguchi et al. (U.S. Patent No. 6,682,965 B1, hereinafter Noguchi); Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Noguchi in view of Watanabe et al. (U.S. Patent No. 5,815,223, hereinafter Watanabe).

Claims 1, 2, and 5 are amended to overcome the objection of paragraph 2 of the Official Action. Claim 1 is further amended to recite that the silicon substrate does not include SiGe. Support for this amendment is found in Applicants' originally filed specification.[1] No new matter is added.

Briefly recapitulating, Claim 1 is directed to a semiconductor device including a polysilicon gate electrode provided on a silicon substrate that does not include SiGe. The polysilicon gate electrode is subjected to compressive stress as internal stress therein, to apply tensile stress to said silicon substrate. Ions having a mass number of 70 or more are implanted into the polysilicon gate electrode. Using ions with a mass number of 70 or more allows for an improvement in carrier mobility and simplified manufacturing.[2]

Noguchi discloses a semiconductor device that includes boron diflouride as a p-type impurity implanted in a strain effect silicon layer 24 on both sides of a gate electrode 73, where gate electrode 73 is used as a mask, to form an n-type source and drain (74 and 75) in

[1] Specification, page 10, line 1 – page 11, line 1.
[2] Specification, page 2, lines 4-12; page 3, lines 17-20.

an upper region of the strain effect silicon layer 24.[3] Also, arsenic as an n-type impurity implanted in a strain effect silicon layer 24 on both sides of a gate electrode 13, where gate electrode 13 is used as a mask, to form an n-type source and drain (14 and 15) in an upper region of the strain effect silicon layer 24.[4] However, Noguchi does not disclose or suggest a silicon substrate that does not include SiGe as recited in Applicants amended Claim 1. That is, Noguchi only discloses a semiconductor device using a strained silicon substrate that includes SiGe (layers 21, 22).

Because Noguchi does not disclose or suggest a silicon substrate that does not include SiGe, Applicants submit that the invention defined by Claim 1, and all claims depending therefrom, is not anticipated and is not rendered obvious.[5] Applicants have also considered Watanabe and submit this reference does not cure the deficiencies of Noguchi.

Accordingly, in view of the present amendment and in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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[3] Noguchi, column 12, lines 25-40; Figure 7c.
[4] Noguchi, column 12, lines 45-60; Figure 7d; see also disclosure relative to Figure 3b.
[5] MPEP § 2142 "...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."